

Amendments to the Claims:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1-16. (Canceled)

17. (Currently Amended) An integrated circuit comprising comprising:

a clock circuit emitting a clock signal;

~~at least a digital part comprising a plurality of transistors connected to one another so as to form a plurality of functional elements, the functional elements being grouped in subassemblies each comprising comprising:~~

a first power supply terminal;

and a second electrical power supply terminal and terminal;

a processor connected between the first and second power supply

terminals; and

a clock input, input coupled to the clock circuit; and

a level shifter connected between the clock circuit and the clock input of at least one of the subassemblies,

wherein the level shifter is configured to adapt the clock signal to a voltage between the first and second power supply terminals of the at least one of the subassemblies, and

the subassemblies being powered are connected in a series arrangement by means of their first and second power supply terminals from between terminals of a voltage supply source, source.

wherein a same clock signal is applied to the clock input of all subassemblies, by a device for shifting the levels of the clock signal.

18. (Currently Amended) The integrated Integrated-circuit according to claim 17,
wherein the clock inputs of at least two adjacent subassemblies are connected by a ~~device for~~
~~shifting the clock signal levels~~the level shifter.

19. (Currently Amended) The integrated Integrated-circuit according to claim 18,
wherein the clock input of an end subassembly is connected by an additional ~~device for~~
~~shifting the clock signal levels~~level shifter at the output of the clock circuit.

20. (Currently Amended) The integrated Integrated-circuit according to claim 17,
wherein the ~~device for shifting the clock signal levels~~level shifter comprises at least one
capacitor.

21. (Currently Amended) The integrated Integrated-circuit according to claim 17,
wherein the ~~device for shifting the clock signal levels~~level shifter comprises at least one
transistor.

22. (Currently Amended) The integrated Integrated-circuit according to claim 17,
wherein all the subassemblies are identical.

23. (Currently Amended) The integrated Integrated-circuit according to claim 17,
wherein each of the subassemblies further comprises a voltage limiting circuit connected
between the first and the second ~~electrical power~~ supply terminals.

24. (Currently Amended) The integrated Integrated-circuit according to claim 23,
wherein the voltage limiting circuit comprises a diode.

25. (Currently Amended) The integrated Integrated-circuit according to claim 23,
wherein the voltage limiting circuit comprises a transistor.

26. (Currently Amended) The integrated Integrated-circuit according to claim 17,
wherein each subassembly further comprises a decoupling capacitor connected between the
first and the second ~~electrical power supply terminals of the subassembly~~terminals.

27. (Currently Amended) The integrated ~~Integrated~~-circuit according to claim 17, wherein the integrated circuit further comprises electrical insulation between the subassemblies.

28. (Currently Amended) The integrated ~~Integrated~~-circuit according to claim 27, wherein the electrical insulation between the ~~different~~-subassemblies comprises reverse biased diode junctions.

29. (Currently Amended) The integrated ~~Integrated~~-circuit according to claim 27, wherein the electrical insulation between the ~~different~~-subassemblies comprises dielectric zones.

30. (Currently Amended) The integrated ~~Integrated~~-circuit according to claim 17, wherein the integrated circuit further comprises silicon blocks from a silicon-on-insulator substrate.

31. (Currently Amended) The integrated ~~Integrated~~-circuit according to claim 17, wherein the subassemblies are at different electrical potentials, and wherein a potential difference between two end subassemblies is greater than a potential difference between terminals of each subassembly.

32. (Canceled)

33. (Currently Amended) The integrated ~~Integrated~~-circuit according to claim 17, wherein ~~the~~ a same current flowing through ~~the~~ different subassemblies varies by less than 20%.

34. (Currently Amended) The integrated ~~Integrated~~-circuit according to claim 17, wherein the subassemblies are formed in such a way that, at all times in operation, ~~the~~ a same current flows through each of the subassemblies.

35. (Currently Amended) A method of controlling current in an integrated circuit comprising:

applying a same clock signal to a clock input of all subassemblies via a device for shifting the levels of the clock signal, level shifter configured to adapt a clock signal emitted from a clock circuit to a voltage between first and second power supply terminals of at least one of the subassemblies, the subassemblies being in a structure in which an integrated circuit comprises at least comprises:

a clock circuit emitting a clock signal;

~~a digital part comprising a plurality of transistors connected to one another so as to form a plurality of functional elements, the functional elements being grouped in subassemblies each comprising~~ comprising:

a first power supply terminal;

and a second electrical power supply terminal and terminal;

a processor connected between the first and second power supply terminals; and

a clock input, input coupled to the clock circuit; and

wherein the level shifter is connected between the clock circuit and the clock input of the at least one of the subassemblies, and

the subassemblies being powered are connected in a series arrangement by means of their first and second power supply terminals from between terminals of a voltage supply source.

36. (Currently Amended) A power supply system for an integrated circuit comprising:

a power supply;

an integrated circuit, the integrated circuit further comprising:

a clock circuit emitting a clock signal;

~~at least a digital part comprising a plurality of transistors connected to one another so as to form a plurality of functional elements, the functional elements being grouped in subassemblies each comprising:~~

~~a first power supply terminal;~~

~~and a second electrical power supply terminal;~~

~~a processor connected between the first and second power supply terminals; and~~

~~a clock input, input coupled to the clock circuit; and~~

~~a level shifter connected between the clock circuit and the clock input of at least one of the subassemblies,~~

~~wherein the level shifter is configured to adapt the clock signal to a voltage between the first and second power supply terminals of the at least one of the subassemblies, and~~

~~the subassemblies being powered are connected in a series arrangement by connecting a second supply terminal of a subassembly to a first supply terminal of a next subassembly in the series arrangement, and connecting the first supply terminal of a first subassembly in the series arrangement and the second supply terminal of a last subassembly in the series arrangement across the power supply; and supply.~~

~~a clock circuit providing an identical clock signal to the clock input of each one of the subassemblies via a device for shifting the levels of the clock signal.~~

37. (New) The integrated circuit according to claim 17, wherein an electrical current flows from a positive terminal of the power supply source to a negative terminal of the power supply source.